School of Electrical and Computer Sciences
Department of Electronics and Communication Engineering

List of shortlisted candidates for the Written Test for Ph.D Admission (Electronics and Communication Engineering) for Spring 2024 – 25

Sl. No.	Application No.	Name	Gender	Category	Whether PwD (Y/N)
1	2024201010699	SWETA MINJ	female	ST	N
2	2024201011282	HEMANT KUMAR	male	SC	N
3	2024201011332	TARUN KUMAR ABHISHEK	male	OB	N
4	2024201111645	SUJATA MAHARANA	female	GE	N
5	2024201111713	RIYA KAUNDAL	female	SC	N
6	2024201211274	CHANDAVATH SUMAN	male	ST	N
7	2024201211288	LAXMIKANT VISHNU SAPKAL	male	GE	N
8	2024201211798	BICKEY LOHAR	male	OB	N
9	2024201311039	RAMAKRISHNA MAHAPATRA	male	GE	N
10	2024201410148	MANASWINI MISHRA	female	GE	N
11	2024201410296	KARANDEEP KAUR	female	SC	N
12	2024201510440	BISHAL LASKAR	male	GE	N
13	2024201510997	DISHI PUROHIT	female	GE	N
14	2024201511087	KAVISHA SINGH	female	GE	N
15	2024201511193	TAPAS ROUT	male	GE	N
16	2024201511446	NITISH DAS	male	GE	N
17	2024201511636	LIPSA SUBHADARSHINI	female	SC	N
18	2024201611440	INGOLE ASHLESHA NILESH	female	GE	N
19	2024201710115	SOUMYASUT RAWAT	male	ST	N
20	2024201710473	SAMARPITA BANERJEE	female	GE	N
21	2024201810631	SHREYANSHI MATURKAR	female	GE	N
22	2024201810790	SHILPI THAWAIT	female	OB	N
23	2024201910502	SHAKTI PRASAD SENAPATI	male	OB	N

Written Test	Interview	Venue
Thursday, 5 December 2024 09:30 – 11:00 AM Reporting time: 08:30 AM	Thursday, 5 December 2024 and/or Friday, 6 December 2024	School of Electrical and Computer Sciences, IIT Bhubaneswar, Argul, Odisha - 752050

Note: Candidates should plan their visit such that they may be expected to be available on BOTH days i.e. 5 December and 6 December 2024. Please see page 2 for more information regarding the written examination.

Information regarding the written examination on 5 December 2024

1. The written examination will be for a duration of 90 minutes i.e. 09:30 – 11:00 AM. Candidates should report at 08:30 AM for their document verification (please see the call letter for details).

2. The written examination will consist of multiple-choice questions, each of 2 marks. There is no negative marking.

3. The written test paper will have two parts: Part A (10 questions), and Part B (15 questions). Part A is common for ALL candidates. It will have questions on Basic Electronics and Circuit Analyses, and Continuous Time Signals and Systems.

4. Part B is specific to the disciple preferred by the candidates. There will be 2 choices: (1) Signal Processing and Communication Engineering (SPCE) and (2) Semiconductor Technology and Chip Design (STCD). You will be asked to indicate your choice of paper at the start of the written examination.

5. For the Part B SPCE paper, there will be questions on Analog and Digital Communications, Digital Signal Processing, and Electromagnetics.

6. For the Part B STCD paper, there will be questions on Electronic Devices, VLSI Design, and Analog and Digital Circuits.

7. The Syllabi for the above subject areas are on similar lines as the GATE examination. For more details, visit: https://gate2024.iisc.ac.in/wp-content/uploads/2023/07/ec.pdf

BEST WISHES