M. TECH

Semiconductor Technology and Chip Design (STCD)

Course Curriculum

School of Electrical and Computer Sciences

IIT Bhubaneswar

January 12, 2026, Version 2.1

Semiconductor Technology and Chip Design

The following table summarizes the structure of the two-year M. Tech program in **Semiconductor Technology and Chip Design** spread across four semesters. Elective subjects are grouped into two baskets, i. e., Elective Basket-I: **Semiconductor Technology** and Elective Basket-II: **Chip Design**. Students are expected to take **at least two electives from each basket**.

Subject Name	Code	L-T-P	Credits	Hours
SEMESTER-I				
Semiconductor Device Modeling	EC6L017	3-0-0	3	3
Semiconductor Device Fabrication	EC6L064	3-0-0	3	3
Analog CMOS VLSI Design	EC6L065	3-0-0	3	3
Digital CMOS VLSI Design	EC6L088	3-0-0	3	3
Semiconductor Packaging and Testing	EC6L063	3-0-0	3	3
Chip Design & Simulation Lab-I	EC6P055	0-0-3	2	3
TCAD, Fabrication & Characterization Lab-I	EC6P056	0-0-3	2	3
Total Credits	19			
SEMESTER-II				
Open Elective-I/Departmental Elective-I		3-0-0	3	3
Departmental Elective-II		3-0-0	3	3
Departmental Elective-III		3-0-0	3	3
Departmental Elective-IV		3-0-0	3	3
Departmental Elective-V		3-0-0	3	3
Chip Design & Simulation Lab-II	EC6P057	0-0-3	2	3
TCAD, Fabrication & Characterization Lab-II	EC6P058	0-0-3	2	3
Thesis Part-1 (Literature review-MTP)	EC6D054		2	
Total Credits	21			
SEMESTER-III				
Thesis Part-II (MTP)	EC6D055		14	
Total Credits	14			
SEMESTER-IV				
Thesis Part-III (MTP)	EC6D056		14	
Total Credits	14			

Semiconductor Technology and Chip Design

Electives Basket-I: Semiconductor Technology				
Subject Name	Subject Code	L-T-P	Credits	Hours
Semiconductor Characterization	EC6L067	3-0-0	3	3
Thin Films Technology	EC6L068	3-0-0	3	3
Advanced Memory Devices	EC6L069	3-0-0	3	3
Advanced Semiconductor Devices	EC6L070	3-0-0	3	3
Power Semiconductor Devices and Technology	EC6L071	3-0-0	3	3
MOS Device Modeling and Characterization	EC6L017	3-0-0	3	3
Quantum Structures and Devices	EC6L073	3-0-0	3	3
Optoelectronic Devices	EC6L074	3-0-0	3	3
Semiconductor Packaging and Testing	EC6L063	3-0-0	3	3
Electives Basket-II: Chip Design				
Subject Name	Subject Code	L-T-P	Credits	Hours
Neuromorphic AI Chip Design	EC6L075	3-0-0	3	3
Digital System Design and Synthesis	EC6L076	3-0-0	3	3
Mixed-Signal VLSI Design	EC6L057	3-0-0	3	3
System-on-Chip Design	EC6L077	3-0-0	3	3
VLSI Physical Design	EC6L078	3-0-0	3	3
RF CMOS SoC Design	EC6L079	3-0-0	3	3
VLSI Digital Signal Processing	EC6L080	3-0-0	3	3
Architecture Design for Digital ICs	EC6L081	3-0-0	3	3
VLSI for Computer Arithmetic	EC6L082	3-0-0	3	3
Fault Tolerant Digital VLSI Systems	EC6L083	3-0-0	3	3
VLSI CAD	EC6L054	3-0-0	3	3
VLSI Testing	EC6L055	3-0-0	3	3
SerDes Systems & Circuits	EC6L062	3-0-0	3	3
Parallel Systems	EC6L060	3-0-0	3	3
VLSI Interconnects	EC6L084	3-0-0	3	3
Digital Design with Chisel	EC6L085	3-0-0	3	3
SystemVerilog for Design and Verification	EC6L086	3-0-0	3	3

Subject Name : Semiconductor Device Modeling

Subject Code	EC6L017	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	No						

Objective of Course: This course will provide a basis for understanding the underlying physics of semiconductor devices, their operation, and their limitation. It is essential to have a thorough insight into semiconductor physics to understand present-day devices and to build future developments in this field. Further, the course will help the students to explore the mathematical modeling of the governed physical phenomenon at the preliminary stage, which can be extrapolated in advanced courses and research in the semiconductor domain.

Syllabus:

Module 1 Semiconductor Physics Overview: Evolution of the devices, Diamond structure of Silicon, Band and Bond Model of the Intrinsic and Extrinsic semiconductor, Energy band diagram of Uniform and Non-uniform doped semiconductor, Carrier Transport: Drift and Diffusion, Mathematical expressions governing the carrier statistics.

Module 2 PN Junction: Overview of the junctions, PN junction under equilibrium, I/V characteristics of the diode: Forward and Reverse, Junction Capacitances.

Module 3 Metal Semiconductor and Heterojunctions: Schottky barrier diode, Metal semiconductor Ohmic contact, Heterojunction: Two-dimensional electron gas.

Module 4 Two terminal MOS Cap: Flat-band voltage, Potential balance and charge balance, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance.

Module 5 Three and Four Terminal MOS: Field Effect Transistor: Three Terminal MOS, Body effect, Four Terminal MOS: Regions of inversion, Transistor regions of operation, General charge sheet model.

Suggested Text/Reference Books:

1. Neaman D. A. “Semiconductor Physics and Devices,” 4th Ed. 2012, McGraw Hill Publication, ISBN 978-0-07-352958-5
2. Streetman B. G. and Banerjee S. K., “Solid State Electronics Devices,” 6th Ed. 2009, PHI Learning Pvt. ltd. Publication, ISBN 978-81 -203-3020-7
3. Tsvidis Y. and McAndrew C, Operation and Modelling of MOS Transistor, 3rd Ed. 2011, Oxford Univ. Press, ISBN 978-0-19-517015-3
4. Mishra U. K. and Singh J. “Semiconductor Device Physics and Design,” 2008, Springer, ISBN 978-1-4020-6480-7
5. S. Karmalkar, ”Solid State Devices,” NPTEL video lectures # 1- 42 and their transcripts available

@ https://nptel.ac.in/courses/117106091

6. S. Karmalkar, "Semiconductor Device Modeling," NPTEL video Modules: 0, 1, 7, 9-14 available @ http://nptel.ac.in/courses/117106033/

Learning Outcomes: At the end of the course, students must be able to

1. Explain the band and bond model of the intrinsic and extrinsic semiconductors.
2. Explain carrier transport mechanism in semiconductors: Drift and Diffusion.
3. Describe the mathematical expression governing carrier statistics.
4. Draw the energy band diagram of the PN junction under equilibrium.
5. Derive the mathematical formulation of PN junction characteristics.
6. Draw I/V characteristics of the diode in both biasing conditions.
7. Explain the possible modes of MOS Cap: Accumulation, Depletion, and Inversion.
8. Draw C/V characteristics of the MOS cap.
9. Explain the three terminal MOS qualitatively.

Subject Name : Semiconductor Device Fabrication

Subject Code	EC6L064	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: This course will cover the science and technology of conventional and advanced microfabrication techniques for electronics, integrated and discrete components. Topics include semiconductor processing, diffusion; ion implantation, thin-film growth including oxides and metals, molecular beam and liquid-phase epitaxy; optical and advanced lithography; and plasma and wet etching, packaging techniques etc. which are the integral components in a conventional fabrication process line. The course will accustom and train the students to a real-time electronic fab environment through the curriculum, activities, industry talks and facility visits.

Syllabus:
Module 1: Introduction to semiconductor and cleanroom substrates processing technology. Thermal oxidation, RTP and furnaces, laser and spike processing. Doping and implantation.
Module 2: Lithography (part 1): fundamentals, contrast, resist, masks, multiple exposure, etc. Lithography (part 2): process, resist, direct write, EBL, proximity, etc.
Module 3: Basics of thin film deposition, PVD (sputtering, evaporation), Epitaxial growth, LPCVD, PECVD, crystallization/recrystallization,
Module 4: Wet etching, Dry etching, Metallization and wire bonding,.
Module 5: Device isolation and packaging Device technology (CMOS, GaAs FET, silicon photonics) Integrated circuit manufacturing (yield, DOE, SPC, etc).
Mandatory sessionals: Expert talks (from industry and academia), group activity, fabrication facility visit

Suggested Text/Reference Books:

1. Stephen A. Campbell, Fabrication engineering at the micro-and nanoscale, 4th Edition, Oxford University Press, 2008
2. Milton Ohring, Materials science of thin films: deposition and structure. Elsevier, 2001
3. Robert F. Pierret, Semiconductor device fundamentals. Pearson Education India, 1996
4. Sunipa Roy, Solid State & Microelectronics Technology. Bentham Science Publishers, 2023

Learning Outcomes: At the end of the course, students must be able to

- Visualize the basic semiconductor device fabrication process steps.
- Correlate and realize the different processes and their sequence that are employed in a foundry.

- Prepare a foundry process wish list.
- Optimize processes based on the design requirements.
- Familiarize with a clean room environment and educate about the dos and don'ts of a semiconductor fab facility.

Subject Name : Analog CMOS VLSI Design

Subject Code	EC6L065	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Electronics/ Introduction to Electronics or equivalent						

Objective of Course: This course builds the basic concepts and the design of advanced CMOS analog Integrated Circuits. This course focuses on the concepts of MOSFETs and the design of amplifiers including non-linear effects. The course will give the practical aspects of CMOS analog IC design. The course aims to teach basic concepts along with advanced design techniques for CMOS amplifiers. The objective of the course is to design and implement the product-level opamps and buffers for VLSI applications.

Syllabus: Introduction to analog VLSI and mixed-signal issues in CMOS technologies; Recapitulation: I-V characteristic of MOS transistors, large signal and small signal models of MOS transistors, device parasitics, feedback configurations and stability theory; Basic MOS models, SPICE models, and frequency-dependent parameters; Amplifiers: Basic amplifier topologies and their characteristics, cascode amplifiers, differential amplifier with active load; Biasing circuits: Simple and cascode current mirrors; Two-stage differential amplifier: Analysis for different performance parameters, pole-zero compensation and design, Operational amplifier design, OTA design; Current reference, voltage reference circuits; Comparator: Simple comparator, switch-based comparator, latch-based comparator; Device mismatch and noise analysis.

Suggested Text/Reference Books:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill Education, Second Edition (2017).
2. CMOS Analog Circuit Design" by Phillip Allen and Douglas R. Holberg, OUP USA; Third Edition edition (1 September 2011)
3. Microelectronic Circuits-Theory & Applications" by A.S. Sedra and K.C. Smith, Adapted by A.N. Chandorkar, 6th Edition, Oxford, 2013

Learning Outcomes: At the end of the course, students must be able to

1. Develop proficiency in designing fundamental analog circuits such as amplifiers (operational amplifiers, voltage amplifiers), current mirrors, voltage references, and filters using CMOS technology.
2. Learn techniques to analyze, minimize, and mitigate noise sources within analog CMOS circuits, ensuring optimal signal integrity and performance.

3. Acquire skills in layout design specific to analog CMOS ICs, focusing on minimizing parasitic elements, achieving symmetry for matched components, and optimizing for performance, area, and manufacturability.
4. Develop the ability to evaluate and make informed decisions regarding trade-offs in analog CMOS IC design, such as speed vs. power consumption, area vs. performance, and noise vs. bandwidth.
5. Apply theoretical knowledge through hands-on design projects that involve the complete design flow of analog CMOS ICs, from initial concept and simulation to layout, fabrication considerations, and verification.

Subject Name : Digital CMOS VLSI Design

Subject Code	EC6L088	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Electronics/ Introduction to Electronics, Digital Electronics						

Objective of Course: In this course, we look at various digital circuit design styles and architectures as well as the issues that designers must face, such as technology scaling and the impact of interconnect. Implementations of basic CMOS logic gates will be discussed first, looking at optimizing the speed, area, or power. The learned techniques will be applied to more evolved designs such as adders and multipliers. The influence of interconnect parasitics on circuit performance and approaches to cope with them are treated in detail. Substantial attention will then be devoted to sequential circuits, clocking approaches, and memories.

Syllabus: Introduction to VLSI Design Flow: Design Hierarchy, VLSI Design Styles, levels of abstraction, challenges of VLSI design

Review of MOS transistors: fabrication, layout, characterization, overlap capacitances, threshold voltage, body effect, I-V characteristics, channel length modulation, scaling, sub-threshold characteristics, leakage current, short-channel effects

CMOS Inverter: DC and transient characteristics; Noise margins and power dissipation

CMOS combinational logic design: Static CMOS logic, CMOS transmission gates, stick diagram and layout, Elmore delay model, delay estimation, parasitic Delay, logical Effort and electrical effort, interconnect delay estimation, gate sizing and buffering, asymmetric gate, skewed gates, ratioless vs ratioed logic, cascode voltage switch logic, arithmetic circuit design

Dynamic circuits: Dynamic logic gates, footed dynamic logic, monotonicity, NORA logic, domino logic

Sequential Logic Circuits: CMOS D-latch and edge-triggered flip-flop, throughput enhancement with pipelining, timing issues of synchronous digital systems, setup time, hold time, timing violations, clock skew, clock jitter

Memories Cells and Arrays: Memory classification, memory architectures, CMOS SRAM and DRAM cell, sense amplifiers, row decoders, control and timing circuitry

Suggested Text/Reference Books:

1. J. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits*, 2^{nd} edition, Prentice Hall, 2003.
2. D. A. Hodges, H. G. Jackson, R. A. Saleh, *Analysis and Design of Digital Integrated Circuits*, 3rd edition, 2003, McGraw-Hill, 2003.
3. S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits*, Tata McGraw Hill, 2003.
4. N. H. E. Weste, D. Harris, A. Banerjee, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4^{th} Edition, Pearson Education India, 2015.

Learning Outcomes: At the end of the course, the student shall be able to:

- Grasp the overview of silicon fabrication and topics relevant to a CMOS process flow.
- Interpret important DC quantities, transient times, and be introduced to CMOS circuit analysis techniques.
- Analyze electrical characteristics of MOS transistors when used as voltage-controlled electronic switches and create logic networks.
- Design static logic gates using fully complementary designs, in addition to variants such as pseudo-nMOS circuits and novel XOR/XNOR networks.
- Analyze charge sharing and charge leakage in various types of CMOS circuit arrangements.
- Perform RC modelling of propagation and contamination delay of gates, RC delay of interconnects, and derive the Elmore formulas for the time constant of an RC ladder.
- Design precharge/evaluate ripple logic and domino logic cascades.
- Design semiconductor memories, static RAM and DRAM with proper architectures and cell configurations.

Subject Name : Semiconductor Packaging and Testing

Subject Code	EC6L063	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: This course focuses on the fundamentals of semiconductor packaging evolution, current technology, and future developments in advanced semiconductor packaging. This course provides an in-depth and intriguing overview of the dynamic world of advanced packaging, including topics such as package assembly, interconnects, substrates, and advanced packaging materials. This course also highlights the testing and reliability aspects of advanced semiconductor packaging. Along with Thermal Management aspects involved in advanced packaging. Furthermore, this course will introduce the opportunities and challenges and provide a clear direction of the requirements for advanced packaging and its uses in the current industry.

Syllabus:

Introduction to Semiconductor Packaging: Definition of packaging and its significance in various industries; Introduction to packaging, and its importance in Modern Electronics provide an overview of the course structure and learning objectives.

Traditional Packaging Technologies: Exploring different packaging technologies, such as leaded and leadless packages, surface mount technology (SMT), and ball grid array (BGA). Discuss the purpose and characteristics of each technology and explain the factors influencing technology selection.

Introduction to Advanced Packaging: Definition of advanced packaging and its importance in meeting evolving technology requirements. Explaining the benefits and challenges associated with advanced packaging. Exploring different integrated technology of advanced packaging technologies, such as 2.5D, and 3D packaging.

Advanced Packaging Interconnects: Discussion on interconnect technologies used in advanced packaging, such as flip chip bumping, solder balls, and through-silicon vias (TSVs). Explanation of the working principles and considerations for each interconnect technology. Highlight their impact on electrical performance and signal integrity.

Advanced Packaging Materials and Substrates: Detail the substrates and materials used in advanced packaging, such as organic substrates, build-up substrates, redistribution layers (RDLs), interposers, and fan-out substrates. Explaining substrates and materials, their properties, fabrication techniques, and performance characteristics. Discussion on the selection criteria for different advanced packaging applications.

Thermal Management in Advanced Packaging: Introduction to the importance of thermal management in advanced packaging. Discussion on various thermal management techniques, such as heat sinks, thermal interface materials (TIMs), and thermal vias. Explanation of the design considerations for effective thermal management.

Testing and Reliability in Advanced Packaging: The testing methodologies and reliability con-

siderations specific to advanced packaging. Discussion on package-level testing, interconnect testing, and reliability testing. Explanation of various failure analysis techniques and strategies for ensuring package reliability.

Future Trends and Emerging Technologies: Discussion on emerging trends in advanced packaging and their potential impact. Insights into future developments and opportunities in the field.

Suggested Text/Reference Books:

1. Fundamentals of Device and Systems Packaging: Technologies and Applications by Rao R. Tummala, McGrawHill Publications
2. Microelectronics Packaging Handbook by Rao R. Tummala, Eugene J. Rymaszewski, and Alan G. Klopfenstein
3. Semiconductor Advanced Packaging by John H. Lau

Learning Outcomes: Upon successful completion of the course, students should be able to:

- Understand the fundamental principles of semiconductor packaging and its significance in the electronics industry.
- Identify and explain the different types of semiconductor packages and their applications.
- Select appropriate materials for packaging based on thermal, mechanical, and electrical properties.
- Describe the various packaging technologies and processes used in the industry.
- Understand the methodologies and equipment used for testing semiconductor devices.
- Analyze and address reliability issues and failure mechanisms in packaged semiconductor devices.
- Explore advanced packaging techniques and emerging trends in the field.
- Apply knowledge of semiconductor packaging and testing to real-world applications and industry challenges.

Subject Name : Chip Design & Simulation Lab-I

Subject Code	EC6P055	L-T-P	0-0-3	Credits	2	Hours	3
Prerequisite	None						

Objective of Course: This course is intended to provide hands-on experience in the design of various CMOS analog and RF active and passive circuits, with emphasis on the full design flow up to layout techniques.

Syllabus:
Introduction to IC design tools (Cadence and Mentor Graphics tool); Transistor Characterization; Design of a Common Source, Common Gate and Common Drain Amplifier; Design of a Differential Amplifier; Current-Mirrors; Design of a single and two-stage Op-Amps; Design of a BGR; Design of a VCO; Design of a LDO; Introduction to layout techniques; Layout of two-stage Op-amp, Design of RF Integrated Circuits like LNA, Mixer, Power Amplifier, RF and Base-band Filters.

Suggested Text/Reference Books:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits McGraw-Hill Education, Second Edition (2017)

Learning Outcomes: At the end of the course, students must be able to

1. Gain proficiency in using industry-standard software tools for chip design simulation
2. Develop the ability to analyze circuit performance through simulation results, including voltage levels, current flows, and signal timings.
3. Gain insights into optimizing circuit designs for performance metrics such as speed, power efficiency, or noise margins, using simulation data to iterate and improve designs.
4. Understand the importance of rigorous verification and validation processes in chip design, ensuring that simulated results match expected theoretical outcomes.
5. Practice documenting simulation setups, results, and analyses in clear and concise reports, adhering to industry standards for technical documentation.

Subject Name : TCAD, Fabrication & Characterization Lab-I

Subject Code	EC6P056	L-T-P	0-0-3	Credits	2	Hours	3
Prerequisite	None						

Objective of Course: To train the students with the necessary skills to perform (1) process level and device level simulation of a wide variety of semiconductor devices and (2) basic silicon processing and device fabrication flow. The students will learn to generate the I-V and C-V characteristics of devices by incorporating the right set of physical models and also realistic parameters and perform hands on training on how a real device is fabricated in a clean room.

Syllabus:

Module 1: Introduction to TCAD; Role of TCAD in semiconductor device development; Range of devices that can be simulated; Types of analyses that can be performed on a device; TCAD tool overview; Basics of finite element analysis and meshing strategies; Basic 2D-structure creation and doping; Numerical solution type; Device simulation and generating necessary output files; Interpreting the runtime environment; Looking "inside" the device (analysing distribution of all relevant quantities throughout the device as well as along selected cutlines); Models and model parameters; I-V and C-V characteristics; Parallel simulation and introduction to workbench; Process simulation.

Module 2: Introduction to cleanroom, Cleanroom protocols, safety and precautions. Introduction to various instruments. Visit to the cleanroom and an introduction to various processes. Introduction to semiconductor manufacturing, wafer production, wafer Identification, wafer handling, wafer cleaning; thermal oxidation and oxide characterization; Patterning and photolithography: use of resist, UV exposure, pre and post baking, developing and resist lift off, etc.; Etching: dry and wet etching; wafer characterization after etching; Metallization.

Suggested Text/Reference Books:

1. Sentaurus Device User Guide, Synopsys, Mountain View, CA, USA, 2015
2. SATLAS User's Manual, SILVACO International, Santa Clara, CA, USA, 2006
3. SGhandhi S K, VLSI Fabrication Principles: Silicon and Gallium Arsenide 2nd Edition, Wiley Blackwell (1994)
4. SPlummer J D, Deal M D and Griffin P B, Silicon VLSI Technology: Fundamentals, Practice, and Modeling,1st Edition, Pearson Education (2009)
5. SSze S M, VLSI Technology, 2nd Edition, McGraw Hill Education (2017)

6. SStanley A. Wolf and Richard N. Tauber, Silicon Processing for the VLSI Era Volume 1-Process Technology Lattice Press, 1999

7. SPeter Van Zant, Microchip Fabrication. McGraw-Hill, 2004

Learning Outcomes: At the end of this lab course, students must be able to:

- Design the 2D and 3D structures of the basic devices, e.g., pn junction diode, MOS cap, and MOSFET.
- Extract and calibrate the I/V and C/V characteristics of the device
- Fabricate the basic MOS capacitor and layered structures.

Subject Name : Chip Design & Simulation Lab-II

Subject Code	EC6P057	L-T-P	0-0-3	Credits	2	Hours	3
Prerequisite	None						

Objective of Course: The purpose of this lab is to instruct students about hardware description languages such as Verilog, and various Verilog modelling issues, such as behavioral and structural modeling and timing simulation. After having introduced Verilog in depth, the possibilities and rapidly growing interest in adaptive hardware and corresponding design techniques shall be introduced by providing the necessary knowledge for understanding and designing reconfigurable hardware systems and studying applications benefiting from dynamic hardware reconfiguration.

Syllabus: Introduction to Hardware Description Language (HDL) such as Verilog, Verilog variables, operators and language constructs, testbenches and simulation, Xilinx FPGA families, Vivado Design Flow, and various FPGA boards, implementation of combinational circuits such as full adders, subtractors, multiplexers, decoders, comparators. Implementation of sequential elements such as latches, flip-flops, and circuits like counters, shift registers, and sequence detectors. Design and optimization of datapath, control and prototyping. Pipelining and memory modeling. Introduction to ZYNQ FPGAs, integration of ARM processors using AHB bus, and control/configuration of FPGA using ARM core. Introduction to Vivado HLS flow and implementation of simple algorithms/designs.

Suggested Text/Reference Books:

1. C. Unsala and B. Tar, *Digital System Design with FPGA: Implementation Using Verilog and VHDL*, McGraw Hill, 2017
2. S. Churiwala (Editor), *Designing with Xilinx FPGAs: Using Vivado*, Springer International Publishing AG, 2016.
3. S. Palnitkar, *Verilog HDL*, 2^{nd} Edition, Pearson India, 2003.
4. S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, 2^{nd} Edition, McGraw Hill Education, 2003.

Learning Outcomes: At the end of this lab course, students must be able to

- Familiarize with hardware description language such as Verilog.
- Implement combinational and sequential circuits
- Optimize designs in accordance to several performance metrics.
- Understand FPGA slice architecture.

- Interpret and analyze post implementation timing simulation.
- Develop knowledge on high level synthesis.

Subject Name : TCAD, Fabrication & Characterization Lab-II

Subject Code	EC6P058	L-T-P	0-0-3	Credits	2	Hours	3
Prerequisite	None						

Objective of Course: TCAD, Fabrication and Characterization laboratory II course will focus on a hands-on experience to a simulate and fabricate any specific device and perform its characterization. The laboratory course will provide a blend of prior knowledge of device simulation platform and basic fabrication step to develop one practical devices. The students will realize the challenges faced during actually realizing one device at from the blue print (simulator) to the wafer level (fabrication) and how to test their efficiency (characterization) and what parameters govern the efficiency.

Syllabus:

Module 1: Recap of the concepts learnt in TCAD, Fabrication and Characterization Lab I; MOSFETs: 2D, 3D, FinFETs and Emerging Devices; Two terminal MOSFET: device design, simulation and understanding the device physics; Device level optimization; Process simulation for the optimized device; Process optimization;

Module 2: Recap of basic fabrication flow concepts learnt in TCAD, Fabrication and Characterization Lab I; Fabrication of a two terminal vertical MOS device; Optimization of the structure based on simulation; Profilometry; Structural characterization: X Ray Diffraction; Morphological characterization: Scanning Electron Microscopy; Band structure analysis: UV-Visible Spectrophotometry; I-V and C-V measurement; Device performance and deviation analysis; Process and structural optimization.

Suggested Text/Reference Books:

1. Ghandhi S K, VLSI Fabrication Principles: Silicon and Gallium Arsenide 2nd Edition, Wiley Blackwell (1994)
2. Plummer J D, Deal M D and Griffin P B, Silicon VLSI Technology: Fundamentals, Practice, and Modeling,1st Edition, Pearson Education (2009)
3. Sze S M, VLSI Technology, 2nd Edition, McGraw Hill Education (2017)
4. Stanley A. Wolf and Richard N. Tauber, Silicon Processing for the VLSI Era Volume 1-Process Technology Lattice Press, 1999
5. Peter Van Zant, Microchip Fabrication. McGrawHill, 2004

Learning Outcomes: At the end of this lab course, students must be able to:

- Design the 2D and 3D structures of the basic devices, e.g., pn junction diode, MOS cap, and MOSFET using SProcess.
- Extract the I/V and C/V characteristics of the devices and perform the reliability test.
- Electrically, optically and morphologically characterize the MOS capacitor.

Subject Name : Semiconductor Characterization

Subject Code	EC6L067	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: This course will create the foundation of electronic materials and device characterization. Characterization is an important aspect of semiconductor process technology to understand the semiconductor and the fabricated device quality, feature dimension, texture, etc. The curriculum would educate the students with the basic understanding of different characterization techniques commonly used by a commercial fab thereby training them to work in a real fab environment. It is designed with a combination of theoretical concepts, activities and frequent lab visits.

Syllabus:

Module 1: Basics of materials characterization: crystallography and electronic structures, Diffraction and scattering (XRD, SAXS, etc.), Diffraction spectrum analysis: Williamson-Hall plot, Scherrer's formula, etc.,

Module 2: Scanning Electron Microscopy (SEM), Physics of image formation, contrast, etc., Transmission Electron Microscopy (TEM): Sample preparation, bright field and dark field imaging, Kikuchi line formation and selected area diffraction analysis, Atomic Force Microscopy (AFM)

Module 3: UV-Visible Spectroscopy, Optical band gap calculation, Photoluminescence (PL) Spectroscopy, Concept of excitation wavelength, analysis of optical defects, etc., X-ray Photoelectron Spectroscopy (XPS), Fourier Transform Infrared Spectroscopy (FTIR)

Module 4: Ellipsometry: Principle of operation, calculation of refractive index and thin film thickness, etc., Profilometry

Suggested Text/Reference Books:

1. B.D. Cullity, Elements of X-ray Diffraction. Addison-Wesley Publishing, 1956
2. J. Goldstein, D.E. Newbury, D.C. Joy, C.E.Lyman,P.Echlin,E. Lifshin, L. Sawyer, J.R. M L Sawyer, J R Michael, Scanning Electron Microscopy and X-ray Microanalysis. ASM Handbooks Online
3. David B. Williams, C.Barry Carter, Transmission Electron Microscopy: A Textbook for Materials Science (4 Vol. Set)

Learning Outcomes: At the end of the course, students must be able to

- Realize the importance of materials and device characterization.
- Correlate the analysis of the characterization data to customize the device fabrication process.

- Optimize the device fabrication process to minimize the number of process steps and maximize efficiency.
- Calculate bandgaps, electron concentrations, doping levels, trap/defect density etc. from the characterization datasets.

Subject Name : Thin Films Technology

Subject Code	EC6L068	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: This course would introduce in depth the thin film deposition and growth processes commonly employed in process fabs. It would deal with the physics of growth and deposition, tools and techniques, their operating conditions and controlling parameters. This course is highly relevant to commercial fab growth and deposition processes and it would train the student adequately to handle commercial deposition tools.

Syllabus: Introduction to thin films, Concept of nucleation and growth, thin film growth models: islanding, 2D growth, S-K growth etc., physical deposition techniques: thermal evaporation, electron beam evaporation, parameterization and calculations, sputtering (DC and RF), vacuum basics, chemical deposition techniques: chemical vapor deposition (CVD): substrate orientation, stoichiometric control, etc., types of CVD, epitaxial growth, Molecular Beam Epitaxy (MBE): stoichiometry control, film characterization: ESCA, thickness monitor, etc., Atomic Layer Deposition (ALD), hydrothermal/solvothermal growth

Suggested Text/Reference Books:

1. Milton Ohring, Materials science of thin films: deposition and structure. Elsevier, 2001
2. Guozhong Cao, Nanostructures and nanomaterials: synthesis, properties and applications. Imperial college press, 2004
3. Robert F. Pierret, Semiconductor device fundamentals. Pearson Education India, 1996

Learning Outcomes: At the end of the course, students must be able to

- Use different thin film deposition and growth techniques for device fabrication.
- Optimization of thin film growth techniques for customized design (defect and thickness control)
- Learn the detailed processes of thin film growth used in the commercial foundries

Subject Name : Advanced Memory Devices

Subject Code	EC6L069	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: This course aims to impart the students the foundational knowledge related to the structure, operation, design considerations, and technological evolution of memory devices. This course is in view of the ever increasing demand for high density, reliable, high speed and cost effective memory devices driven by the advent of advanced applications such as 5G, AI, IOT etc.

Syllabus:
Module 1: Introduction to memory devices: Evolution and history.
Module 2: Non-volatile memory devices: Magnetic memories, HDDs; Silicon based thin film transistor non-volatile memories. NAND Flash memory: device structure and architecture, read, write, verify and erase operations and corresponding biasing schemes; Single Level Cell (SLC), Multi-LC, Triple-LC and Quadruple-LC; Vt tightening techniques; Incremental Step Pulse Program; Programming time versus read window budget (RWB) trade-off; Scaling challenges: data retention, cell current fluctuation; Reliability, cycling endurance, read/write disturb, data retention.
Module 3: Volatile memory devices: Random access memories; SRAMs; DRAMs; Development and advancements of DRAM technology, DDR variants; High Bandwidth Memory (HBM).
Module 4: Emerging memory technologies: Phase Change Memory (PCM); Magneto-resistive Random Access Memory (MRAM); Ferroelectric Random Access Memory (FeRAM), Resistive Random Access Memory (RRAM); Comparison and future direction towards universal memory concepts.

Suggested Text/Reference Books:

1. S. Aritome, NAND Flash Memory Technologies, 1st ed., 2016, Wiley-IEEE Press, Hoboken, NJ, USA, ISBN: 978-1119132608
2. S. Raoux and M. Wuttig, Eds., Phase Change Materials: Science and Applications, 1st ed., 2011, Springer-Verlag New York Inc., New York, USA, ISBN: 978-1441946591

Learning Outcomes: At the end of the course, students must be able to

1. Explain the operation of magnetic memories, HDDs, and silicon based thin film transistor non-volatile memories.
2. Explain the physics behind the programming and erase operations of a 3D-NAND cell.
3. Sketch the bias waveform during read, write and erase operation of a 3D-NAND pillar.
4. Estimate the threshold voltage shift of NAND cell during erase and program operation

5. Sketch and explain the concept of pillar potential boost, its role in preventing read/write disturb, and its dependency on material parameters and biasing scheme.
6. Explain the tradeoff between read window budget and programming time.
7. Sketch the bias waveform for ISPP and explain its role in preventing data corruption and ensuring high density data storage.
8. Explain the various types of DRAM and its operation.
9. Explain the operation of PCM, MRAM, FeRAM,and RRAM.

Subject Name : Advanced Semiconductor Devices

Subject Code	EC6L070	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Semiconductor Devices						

Objective of Course: This course provides detailed insight into the advanced semiconductor devices concerning the nanometre dimension regime. The course offered the feasibility of discussion and research on emerging devices and material engineering to improve/overcome the shortcomings of conventional MOSFETs.

Syllabus:

Module 1 Second Order Effects (Short Channel Effects): CMOS scaling theory, Velocity Saturation, Mobility effects, Temperature effects, Channel Length Modulation, Subthreshold conduction, High-k dielectric, DIBL, GIDL, Hot carrier effects

Module 2 SOI Technology: Requirements of high-performance nanoscale devices, Silicon-on-insulator: FDSOI and PDSOI, Subthreshold swing

Module 3 Multi-gate Transistors: FinFET, Gate-all-around, Mobility in Multigate MOSFETs, Radiation effect in multi-gate FETs

Module 4 Ferroelectric Transistors and Stacked Transistors: Feature, Principle and Development of Ferroelectric transistors, Doped-ferroelectric layer, FeFET memory, Idea of Negative Capacitance FET. Concept of area scaling and channel stacking, General properties, and ideas about Nanosheet and Forksheet FET, Complementary FET, and their circuit applications

Module 5 Reliability issues in Emerging Devices: Self-heating effect, Work function variations, Metal grain granularities (MGG), Random dopant fluctuation (RDF), Line edge roughness, Early aging

Suggested Text/Reference Books:

1. Tsvidis Y. and McAndrew C, Operation and Modelling of MOS Transistor, 3rd Ed. 2011, Oxford Univ. Press, ISBN 978-0-19-517015-3
2. Colinge J. P., "FinFET and Other multi-gate transistor, 2008, Springer, ISBN 978-0-387-71751-7
3. Yoon S. M, "Ferroelectric gate Field effect transistor, device physics and application, 2020, Springer

Learning Outcomes: At the end of the course, students must be able to

1. List the various second-order effects of the conventional MOSFET and explain their impact on electrical characteristics.

2. Describe the advantage of SOI technology over bulk-MOSFET.
3. Sketch the multi-gate transistors and explain their geometry effects.
4. Derive the mathematical formulation of the sub-threshold slope for Ferroelectric FETs and explain the negative capacitance phenomenon.
5. Qualitatively explain the possible reliability challenges of the emerging devices and their possible solutions.

Subject Name : Power Semiconductor Devices and Technology

Subject Code	EC6L071	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: This course aims to impart the students the foundational knowledge related to the operation, modeling, design, fabrication, and characterization of power semiconductor devices. It also aims to impart power device simulation and analysis skills through a TCAD based course project. This course is in view of the ever increasing demand for low-loss, robust, reliable, and affordable semiconductor devices with high voltage withstanding capability driven by the growing demands for power-hungry applications including data centers, electric vehicles, electric weaponries, solar and other non-renewable energy etc.

Syllabus:

Module 1: Introduction and overview of power electronic applications; Role of power devices in power electronic circuits; Types of power devices; Switching waveform of an ideal and real power switch; Specifications of interest.

Module 2: Review of basics of semiconductor device physics, p-n junction; Mobility and lifetime; Carrier transport under extreme conditions: electric field, temperature and radiation; Avalanche breakdown.

Module 3: Two terminal power diodes: P-N, Schottky, and P-i-N diodes; Physics of power diodes, Power diode design; Breakdown voltage versus ON-resistance trade-off; Techniques to improve the trade-off: wide band gap semiconductors and super-junction diodes; Edge termination techniques; Thermal considerations and heat sink design; Fabrication of power diodes, and superjunctions in silicon and SiC: challenges and solutions.

Module 4: Three terminal unipolar power devices: VDMOS, UMOS, DMOS, LDMOS; Process flow; Discrete (vertical) versus On-chip devices (lateral); High power MOS design essentials, breakdown voltage and on-resistance modeling, parasitic capacitance and resistances, switching characteristics; Negative differential resistance (NDR), and self-heating. Characterisation of power MOSFETs: unclamped inductive switching (UIS), double pulse testing (DPT), short circuit testing, radiation hardness; State-of-the-art SiC devices and ongoing research.

Three terminal bipolar power devices: IGBT, Thyristor; structure, operation, and fabrication

Suggested Text/Reference Books:

1. B. J. Baliga, Fundamentals of Power Semiconductor Devices,Ed.2, 2019, Springer, ISBN: 978-3-319-93987-2

2. F. Wang, et al., Characterization of Wide Bandgap Power Semiconductor Devices, 1st ed., 2018, IET, London, UK, ISBN: 978-1-78561-491-0

3. S. K. Ghandhi, Semiconductor Power Devices: Physics of Operation and Fabrication Technology, 1st ed., 1977, Wiley, New York, USA, ISBN: 978-0471029991

Learning Outcomes: At the end of the course, students must be able to

1. Sketch the switching characteristics of power devices and estimate the conduction and switching losses.
2. Calculate the breakdown voltage and specific on-resistance of a 1-D junction for a given set of device parameters.
3. Derive the relationship between breakdown voltage and specific on resistance of 1-D junction and superjunction.
4. Design the edge termination structure for a given power diode.
5. Sketch and explain the fabrication process of power diodes and superjunctions.
6. List the various components of the specific on-resistance of a power MOSFET and estimate each of them as a function of device parameters.
7. Design power diodes and MOSFETs for a target breakdown voltage.
8. Sketch the UIS, DPT and short circuit test circuits and explain the operation of the device during these tests.

Subject Name : MOS Device Modeling and Characterization

Subject Code	EC6L072	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: This course will focus on the physics of operation, art of modelling, and techniques of characterization, of Metal-Oxide-Semiconductor (MOS) based junctions/devices. As MOS junctions are an integral part of a wide range of modern devices including planar MOSFETs, FinFETs, NAND flash memory cells, power MOSFETs etc., this course aims to lay the necessary foundation for students to analyze, design and characterize MOS junctions in semiconductor devices for a wide spectrum of applications.

Syllabus :

Module 1: Introduction and overview of MOS junction in modern devices. Contact Potential. P-N junction versus M-S junction. Ideal MOS physics, regions of operation and threshold voltage using surface potential model. C-V measurement setup and characteristics. Real MOS physics: effect of metal work function and oxide and interface trapped charges on threshold voltage and C-V characteristics. MOS parameter extraction from C-V Characteristics.

Module 2: Three terminal MOS structure and operation. Body bias effects. MOSFET: device structure, operation, field-dependent mobility, ID-VDS and ID-VGS derivation and characteristics, short channel and narrow width effects, thin gate-oxide effects, drain series resistance, parameter extraction from I-V characteristics.

Suggested Text/Reference Books:

1. Y. Tsividis and C. McAndrew, Operation and Modeling of The MOS Transistor, 3rd ed., 2010, Oxford University Press, Oxford, UK, ISBN: 978-0195170153
2. B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 6th ed., 2006, Prentice Hall India, New Delhi, India, ISBN: 978-0131497269
3. M. S. Tyagi, Introduction to Semiconductor Materials and Devices, 1st ed., 1991, John Wiley Sons, New York, USA, ISBN 978-8126518678

Learning Outcomes: At the end of the course, students must be able to

1. Sketch the cross sectional and top view of a MOS and MOSFET.
2. Draw and explain the circuit schematic used to obtain the C-V/I-V characteristics of a MOS/-MOSFET.

3. Estimate the threshold voltage of an ideal and real MOS.
4. Sketch the C-V characteristics of a MOS for a given set of device dimensions, gate metal workfunction, semiconductor type and doping, fixed oxide charge, trap type and concentration, frequency of signal source and ambient temperature.
5. Estimate the MOS/MOSFET parameters from the given C-V/I-V characteristics.
6. Sketch and explain the I_D-V_{DS} and I_D-V_{GS} characteristics in both linear and log scale.
7. List and explain the approximations used in deriving the SPICE levels 1 - 4 models.
8. Estimate the electron mobility in the channel for a given set of device parameters, temperature and biasing condition.
9. Explain the various short-channel effects using suitable plots or diagrams.
10. Explain the narrow-width effects in LOCOS and STI-isolated MOSFETs.
11. Estimate the drain current in the presence of series source/drain resistance.

Subject Name : Quantum Structures and Devices

Subject Code	EC6L073	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: With increasing miniaturization, there is a dire need to know about the physics and electronics of sub-micron features. This course introduces the students to the variations in properties encountered in the nanometric levels, the physics behind such variation and devices which exploit such variations for performance enhancement. The course has two modules, the first one deals mostly with fundamental physics of sub micron features while the second part deals with their applications as nanodevices.

Syllabus :

Module 1: Nanostructures: Introduction to quantum science: Heisenberg's uncertainty principle, Schrodinger Wave equation (time dependent and time independent), Quantum well concept (infinite potential wells), quantum confinement, energy discretization, Density of States (DOS): basic concept, DOS calculation for 0D, 1D, 2D and 3D structures, origin of band structure: Hydrogen atom problem, Linear Combination of Atomic Orbitals (LCAO), Effect of size on different physical and electronic parameters: electrical conductivity, melting point, etc., Effect of structure on physical parameters,

Module 2: Nanodevices Finite potential well and concept of tunneling, superlattice, quantum cascade laser (QCL), concept of Coulomb blockade, Coulomb staircase, single electron transistor (SET), concept of valley electrons, spin states and Zeeman effect, qubit generation, basic spin device

Suggested Text/Reference Books:

1. David J. Griffiths, and Darrell F. Schroeter. Introduction to quantum mechanics. Cambridge university press, 2018
2. George W. Hanson, Fundamentals of nanoelectronics. Pearson Education, 2019

Learning Outcomes: At the end of the course, students must be able to

- Develop and solve basic quantum mechanical problems.
- Calculate the generalized electronic band structures using LCAO theory.
- Calculate the variation of electrical and physical parameters for semiconductors.
- Realize the working of quantum devices.
- Understand the basics and operation of spintronic devices.

Subject Name : Optoelectronic Devices

Subject Code	EC6L074	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: This course aims to provide students with an understanding of various semiconductor and non-semiconductor-based optoelectronic devices (light emitters, detectors, etc.). The expected outcomes from the course are: (i) understand the basic working mechanism of the devices, (ii) understand the governing equations to be able to perform calculations to characterize the performance of the devices and, (iii) have the practical knowledge and an understanding of the trade-offs when using these devices in their respective applications.

Syllabus:

Introduction to solid: crystal structure, periodicity in crystals, the origin of defects and their types, carriers in semiconductors, carrier generation-recombination, optical materials, and bandgap engineering, optical properties of materials, drift, diffusion, and continuity equation. Photoelectric devices: photodetectors, & LEDs, optical pumping and avalanche multiplication, lasers, organic LEDs, and the concept of optical bandgaps. Optoelectronic instrumentation: UV/Visible, PL, etc. Beer-Lambert's Law, Photovoltaic devices.

Suggested Text/Reference Books:

1. Photonics: Optical Electronics in Modern Communications, Amnon Yariv & Pochi Yeh
2. Fundamentals of Photonics, B.E.A. Saleh & M.C. Teich
3. Building Electro-optical systems and making it all work, P.C.D. Hobbs

Learning Outcomes: At the end of the course, students must be able to

- Understanding the periodicity of crystals and role of defects in generating optical properties in semiconductors.
- Draw the band structure and I-V characteristics of different optical devices.
- Using the optical characterization instruments to analyse opto-electronic devices.
- Implement the drift-diffusion model and continuity equation to understand the working of real-time opto-electronic devices.

Subject Name : Neuromorphic AI Chip Design

Subject Code	EC6L075	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Basic Electronics / Introduction to Electronics						

Objective of Course: Students will demonstrate the tradeoffs between various neuromorphic implementations starting at a fundamental circuit level through larger system design. Demonstrate analytical modeling of neuromorphic blocks, including the various aspects of computational neuroscience and analog electrical modeling and the relationships between these blocks and will demonstrate utilizing computer design tools and experimental measurement opportunities in the design of neuromorphic architectures, as well as in the design of full analog systems.

Syllabus: Introduction to Neuromorphic Engineering; Signalling and operation of Biological neurons, neuron models, signal encoding and statistics; Synapses and plasticity rules, biological neural circuits; Neuromorphic design principles; FETs - device physics and sub-threshold circuits; Analog and digital electronic neuron design; Non-volatile memristive semiconductor devices; Electronic synapse design; Interconnection Networks; Interconnection schemes for large non-spiking and spiking neural networks; Analysis of design, architecture and performance characteristics of demonstrated chips employing Analog neuromorphic VLSI, Digital neuromorphic VLSI, Electronic synapses and other neuromorphic systems. Neuromorphic Systems, Electronic Cochlea, Auditory Localization, Silicon Retinas: Voltage and Current Mode, Neuron Models, Address Event Communication and Motor Pattern Generation.

Suggested Text/Reference Books:

1. Shih-Chii Liu, Jörg Kramer, Giacomo Indiveri, Tobias Delbrück, Rodney Douglas, Analog VLSI: circuits and principles, MIT press, 2002, ISBN 0262122553
2. Carver Mead, Analog VLSI and neural systems, Addison-Wesley, 1989, ISBN0201059924
3. Eric Kandel, James Schwartz, Thomas Jessell, Steven Siegelbaum, A.J. Hudspeth, Principles of neural science, McGraw Hill 2012, ISBN 0071390111
4. Dale Purves, Neuroscience, Sinauer, 2008, ISBN 0878936971

Learning Outcomes: At the end of the course, students must be able to

- Gain a deep understanding of the principles and mechanisms underlying biological neural systems, including neuron behavior, synapse dynamics, and network organization.

- Learn various neuromorphic models and algorithms used to simulate neural behavior in silicon, including spiking neural networks (SNNs), rate-based models, and learning algorithms like spike-timing-dependent plasticity (STDP).
- Develop skills in designing and implementing neuromorphic circuits using VLSI techniques, including analog and digital circuit design, mixed-signal integration, and layout considerations.
- Understand the architecture and organization of neuromorphic chips, including the arrangement of neurons, synapses, and connectivity patterns optimized for efficient computation and communication.
- Explore techniques for optimizing energy efficiency in neuromorphic VLSI designs, leveraging principles such as event-driven computation and sparse coding to reduce power consumption.

Subject Name : Digital System Design and Synthesis

Subject Code	EC6L076	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Digital Electronics						

Objective of Course: This course introduces the students to state-of-the-art design methodologies through practical design applications. Students will learn and design complete systems with FPGAs that includes coding, testing, synthesizing and implementation. In this process, students will also learn the best coding practices, and optimize the design for performance, area, and power. The main objective of the course is "Learn by doing rather than just reading". Students will also get a chance to try and experiment a lot through the assignments and term project.

Syllabus: Advanced topics in combinational and sequential design: Use of CAD, design methodologies, system decomposition, arithmetic modules, and design of complex sequential systems. Introduction to FPGA architectures: Overview, programming technologies, configurable logic block, FPGA routing architectures. Logic design with Verilog: Introduction to Verilog, logic design with behavioral models of combinational and sequential logic, synthesis of combinational and sequential logic, design and synthesis of data path controllers, programmable logic and storage devices, algorithms and architectures for digital processors, architectures for arithmetic processors, coding for FPGAs. Designing with FPGAs: Design flow for FPGAs, prototyping with FPGAs, and debugging. (Utilize commercial FPGA development tools for compilation, simulation, synthesis, implementation, and debugging).

Suggested Text/Reference Books:

1. M. Ciletti, *Advanced digital design with the Verilog HDL*, Prentice Hall Upper Saddle River, 2003.
2. S. Palnitkar, *Verilog HDL: a guide to digital design and synthesis*, Prentice Hall Professional, 2003.
3. C. Unsalan, B. Tar, *Digital system design with FPGA: Implementation using Verilog and VHDL*, TMH, 2017.
4. Steve Kilts, *Advanced FPGA Design: Architecture, Implementation, and Optimization*, Wiley, 2007
5. Richard C. Dorf, John V. Oldfield, *Field-Programmable Gate Arrays: Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems*, Wiley, 2008

Learning Outcomes: Upon successful completion of the course, students should be able to:

- Design basic combinational and sequential logic circuits.

- Develop Verilog code for various digital circuits and simulate and debug Verilog designs using simulation tools.
- Synthesize Verilog designs to create gate-level representations and understand the synthesis process and constraints.
- Understand the coding styles to realize latches, flip-flops, synchronous and asynchronous resets.
- Synthesize designs with FFs with only D inputs or with/without asynchronous pins, and understand the nuances in synthesizing the circuits.
- Understand the simulation versus synthesis issues.
- Use FPGA development boards to implement and test digital designs.
- Get an brief overview of FPGA architectures and how synthesized circuits are realized on FPGAs.

Subject Name : Mixed-Signal VLSI Design

Subject Code	EC6L057	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Analog IC Design						

Objective of Course: Focuses on analog-to-digital and digital-to-analog converters in CMOS technologies. Course content includes discussions of applications, appropriate system specifications, circuit elements, topology tradeoffs, and history.

Syllabus: Sampling theory and discrete-time signals; sample-and-hold circuits; Switch design and switched capacitor circuits; Comparators; Basics of data converters; quantization, ADC and DAC metrics; Nyquist rate ADC's: SAR and pipelines ADC's; Nyquist rate DACS's; Architectures and design of Nyquist rate DAC's; High-resolution data converters (sigma-delta data converters); Mixed-signal layout design; Integrated power management units (Bulk Converter and LDO); Selected topics in mixed-signal VLSI circuits

Suggested Text/Reference Books:

1. Data Conversion System Design, by B. Razavi, IEEE Press, 1995
2. Tony Chan Carusone David A. Johns Kenneth W. Martin, Analog Integrated Circuit Design, Wiley, Second Edition 2011
3. Understanding Delta-Sigma Data Converters, by R. Schreier and G.C. Temes, IEEE Press/Wiley, 2004
4. Data Converters, F. Maloberti, Springer, 2007
5. Analog-to-Digital Conversion, M. Pelgrom, second ed., Springer, 2013
6. Journals and Conferences papers from IEEE SSCS, and IEEE CAS Societies.

Learning Outcomes: At the end of the course, students must be able to

- Explain basics of data converter and its specifications.
- Design and analyze different types of data converters like flash, pipeline, SAR and sigma delta ADCs.
- Design and analyze different types power converters.
- Design and analyze other mixed-signal blocks of SoCs like PLL, etc.

Subject Name : System-on-Chip Design

Subject Code	EC6L077	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Digital Electronics						

Objective of Course: The objective of this course is to impart a general understanding of the structure and operation of systems-on-chip. Main building blocks of a system-on-chip, e.g., processor, on-/off-chip memories, interconnect is introduced. Implementation methods as well as techniques for low power consumption are addressed.

Syllabus: This course provides basics, current trends and challenges in the development of digital system-on-chip (SoC). We start with the main steps for building arbitrary CMOS-based combinatorial logic and sequential digital data processing and control circuitry (e.g. Finite State Machines) and explaining their role and significance in the scope of key system-on-chip components: microprocessors, memories and interconnects. The microarchitectural structure and building blocks of processor elements (RISC cores), on-/off-chip memory technology (SRAM, DRAM, Flash), bus and point-to-point interconnect standards (Processor Local Bus, Advanced Microcontroller Bus Architecture, FIFO) as well as the design of communications specific arithmetic blocks (adder, multipliers, shift and comparators) will be introduced and analyzed. Finally, we will introduce the main implementation methods for SoCs, such as FPGA, standard cell and full custom design, and discuss methods for low-power design, which is vital for the development of SoCs in embedded systems.

Suggested Text/Reference Books:

1. S. Furber, *ARM system-on-chip architecture*, Pearson Education, 2000.
2. V. Chakravarthi, S. Koteshwar, *System on Chip (SOC) Architecture: A Practical Approach*, Springer Nature, 2023.
3. J. Yiu, *System-on-Chip Design: With Arm® Cortex-M Processors: Reference Book*, Arm Education Media, 2019.
4. J. Rabaey, A. Chandrakasan, B. Nikolic, *Digital integrated circuits*, Prentice hall Englewood Cliffs, 2002.
5. W. Wolf, *Modern VLSI Design: IP-Based Design*, Pearson Education, 2008.

Learning Outcomes: Upon successful completion of the course, students should be able to:

- Explain the components and architecture of a typical SoC.
- Discuss the design methodologies and flow used in SoC development.

- Understand different processor architectures and their applications, integrate processor cores into an SoC design.
- Understand various types of memory subsystems, understand their hierarchy, know-how of cache memory and memory management interfaces.
- Design and implement interconnects and buses for on-chip communication.
- Utilize standard communication protocols or peripheral devices, understand their operation, and integration into an SOC.
- Design and implementation of SOCs using FGPA development boards.

Subject Name : VLSI Physical Design

Subject Code	EC6L078	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: The course will introduce the participants to the basic design flow in VLSI physical design automation, the basic data structures and algorithms used for implementing the same. The course will also provide examples and assignments to help the participants to understand the concepts involved, and appreciate the main challenges therein. At the end of the course, the students will be able to a) analyze different algorithms for partition, b) analyze to place and partition the blocks while for designing the layout for IC, c) solve the performance issues in circuit layout, d) analyze the problem formulations for clock-tree routing, and e) analyze the timing and performance constraints.

Syllabus: Introduction to physical design automation.
Partitioning: Kernigham-Lin's algorithm, Fiduccia Mattheyes algorithm, Krishnamurty extension, multilevel partition techniques
Floorplanning: Hierarchical design, wirelength estimation, slicing and non- slicing floor plan, polar graph representation, operator concept, Stockmeyer algorithm for floor planning, mixed integer linear program
Placement: Placement Techniques- Simulated annealing, partition-based, analytical, and quadratic; Timing and congestion considerations
Grid Routing and Global Routing: Introduction and optimization goals, Single net routing (Rectilinear routing), global routing in the connectivity graph, finding shortest paths with Dijkstra's algorithm, full-netlist routing
Detailed Routing: Introduction, channel routing algorithms, switchbox and over the cell routing
Clock Design, Clock tree routing, clock tree synthesis and Power/Ground routing
Static Timing Analysis and Timing Closure: Timing driven placement and routing, zero slack algorithm Physical Synthesis and Performance Driven Design Flow: Interconnect Modeling and Layout Compaction.

Suggested Text/Reference Books:

1. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu, *VLSI Physical Design: From Graph Partitioning to Timing Closure*, Springer, 2011
2. Naveed A. Sherwani, *Algorithm for VLSI Physical Design Automation*, 3rd Edition, Springer, 1998
3. Sung Kyu Lim, *Practical Problems in VLSI Physical Design Automation*, Springer, 2008

Learning Outcomes: Upon successful completion of the course, students should be able to:

- Explain the steps involved in the physical design process.
- Understand design partitioning and floorplanning.
- Understand placement strategies to optimize timing and routability, underlying algorithms.
- Develop deeper understanding of global and detailed routing using appropriate algorithms.
- Understand interconnect and their modeling, including static timing analysis.
- Understand clock tree design, routing, various topologies, and optimizing clock tree for timing, area, and power.

Subject Name : RF CMOS SoC Design

Subject Code	EC6L079	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Analog IC Design						

Objective of Course: Modern integrated wireless communication systems have fundamentally changed the way we live our everyday life, and they will become even more important in the future. Extensive research is underway in the next generation wireless communication systems such as in spectrum sharing, 5G radios, radios for the internet-of- things (IoT's) and millimetre wave transceivers for communication and sensing with the help of scaled CMOS technology. The goal of this course is to convey a methodical design approach for the design of Integrated Circuits for Wireless Communications. The course introduces the principles, analysis, and design of CMOS radio frequency integrated circuits (RFIC) for wireless communication systems. Besides system level design considerations for RF IC, this course also provides the rule-of-thumb approach in designing main RF blocks. A part of the course consists of term projects using modern VLSI design software and foundry RF models.

Syllabus: Introduction to wireless/RF CMOS IC Design: Acronyms, Applications, RF viewpoints, definitions and wireless specifications. System Architecture for Wireless Transceivers: Superheterodyne, homodyne/direct-conversion, sliding-IF architectures etc., Wireless Communication Standards: WLAN, IoT, LTE, 5G, 5G-NR, Bluetooth, I-IoT, NB-IoT etc., Low-Noise Amplifiers: LNA Trade-offs, design requirements, different circuit topologies, matching, inductors design. Mixers: up-conversion and down-conversion mixers, mixer fundamentals and characterization, image rejection, up-conversion and down-conversion mixer circuit topologies, phase-shifters, sampling mixers, subsampling mixers. Introduction to Power Amplifiers: design requirement, approaches, circuit topologies, digital direct synthesis, examples. Clocking Circuits: Oscillators, phase-locked loops, Frequency Synthesizers-Introduction to Fractional-N and Integer-N frequency synthesizers, Study of few complete single-chip RF transceivers, system-to-circuit design examples for a reference wireless standard.

Suggested Text/Reference Books:

1. B. Razavi, RF Microelectronics, 2e Paperback – 1 January 2013, Pearson Education India; 2nd edition (1 January 2013), ISBN-13: 978-9332518636
2. Thomas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press; 2nd edition (22 December 2003).
3. Gu, Qizheng, RF System Design of Transceivers for Wireless Communications, Springer, 2005, ISBN 978-0-387-24162-3
4. Gabriele Manganaro and Domine Leenaerts, Advances in Analog and RF IC Design for Wireless Communication Systems, 2013, Elsevier Inc., ISBN 978-0-12-398326-8

Learning Outcomes: At the end of the course, students must be able to

- Learn advanced modeling techniques for CMOS transistors at RF frequencies, including parasitic elements, non-linear effects, and high-frequency behavior.
- Develop skills in designing RF front-end circuits such as low-noise amplifiers (LNAs), mixers, oscillators, and power amplifiers using CMOS technology.
- Acquire knowledge of specialized techniques for designing high-frequency circuits in CMOS, including layout considerations, parasitic capacitance management, and noise minimization.
- Learn strategies for optimizing noise figure, linearity, and dynamic range in RF CMOS ICs, including trade-offs between power consumption, noise performance, and circuit bandwidth.
- Gain proficiency in using RF simulation tools and equipment for characterizing and validating RF CMOS circuits, including simulation of S-parameters, noise figure, and harmonic distortion.

Subject Name : VLSI Digital Signal Processing

Subject Code	EC6L080	L-T-P	3-1-0	Credits	4	Hours	4
Prerequisite	Introduction to Electronics, Digital Electronics						

Objective of Course: This course will cover the most important methodologies for designing custom or semi-custom VLSI systems for some typical digital signal processing applications. Students will get to learn, how to map DSP algorithms into VLSI efficiently. Several high-level algorithm and architecture design techniques will be introduced that enable joint optimization across the algorithmic, architectural, and circuit domains. General techniques covered include pipelining, retiming, folding and unfolding, and systolic array design. Mapping of algorithms on array structures, DSP systems, and Field Programmable Gate Arrays (FPGAs) will be described for selected algorithms.

Syllabus:

1. VLSI design issues for signal processing and communication algorithms: Mapping of signal processing algorithms into architectures, concepts of pipelining and parallel processing, latency and throughput, graphical representation of DSP algorithms- signal flow graph, data flow graph (DFG) and dependence graph (DG), concept of critical path
2. Retiming: Retiming theorem, forward path and loop retiming, loop bound, iteration bound, fine grained pipelining, Cutset retiming, Retiming IIR Filters, Algorithm for computing iteration bound.
3. Unfolding: Parallel processing in DSP by unfolding, Unfolding by a factor- J, design issues of retiming before unfolding to arrest critical path, unfolding a loop, loop bound and iteration bound calculations, combination of pipelining and parallel processing, bit serial processing, digit serial processing, bit parallel/word serial processing, unfolding of switches and bit serial systems. Partial arrest of hardware overhead on unfolding through suitable DSP tricks: parallel FIR filtering, polyphaser decomposition of sequences, 2-phase and 3-phase (polyphase) decomposition of sequences, hardware efficient 2-parallel and 3-parallel FIR filters.
4. Folding: Folding transformation, concepts of folding factor, scheduling, folding order, folding set. Register minimization techniques: lifetime analysis of variables, forward backward register allocation, delay folded realization of a digital filter.
5. Systolic Arrays: Concepts of N-dimension space, scheduling, projection vector, hardware utilization efficiency (HUE). FIR systolic arrays. Reduced dependence graph, Regular Iterative algorithm, affine scheduling.
6. Bit Level Arithmetic and Architectures: Two's complement representation, Horner's rule, parallel carry ripple and carry save array architecture for multiplication, Lyon's bit serial two's complement multiplier and its pipelined architecture, Concept of canonic signed digit representation, Bit serial FIR and IIR Filter
7. Distributed Arithmetic: Reduce multipliers using concepts of sum-of-power-of-two and ROM, offset

binary coding
8. Redundant Arithmetic: Signed digit number system, carry-free radix-2 addition and subtraction, hybrid radix-2 and radix-4 addition, Redundant to non-redundant converters
9. Numerical Strength Reduction: Subexpression elimination, subexpression sharing, multiple constant multiplication

Suggested Text/Reference Books:

1. K. K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Wiley, NY, 1999
2. M. Mehendale and S. D. Sherlekar, *VLSI Synthesis of DSP Kernels, Algorithmic and Architectural Transformations*, Springer, 2001.
3. L. Wanhammar, *DSP Integrated Circuits*, Academic Press Inc., 1999.
4. M. A. Bayoumi, *VLSI Design Methodologies for Digital Signal Processing Architectures*, Springer, 1994.

Learning Outcomes: At the end of the course, the student shall be able to:

- Realize efficient digital VLSI architectures for signal processing applications.
- Optimize the implementation of signal processing algorithms with respect to speed, area and power, or achieve a suitable trade-off among them.
- Apply various formal techniques and high-level transforms to map signal processing algorithms onto hardware.
- Formulate algorithms for VLSI optimized implementation, governed by the nature of the mathematical equation to be implemented in hardware.

Subject Name : Architecture Design for Digital ICs

Subject Code	EC6L081	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Digital Electronics						

Objective of Course: The course provides an essential background to the architectural design of VLSI, VLSI design flow, and general design methodologies. It will include different aspects of algorithm to architecture mapping, timing analysis and hierarchical system design. It will also cover high performance VLSI architecture design of computer arithmetic algorithms.

Syllabus: VLSI design flow: VLSI design styles: Full custom, standard cell based, gate array based, programmable logic, field programmable gate arrays etc., design automation, design space exploration Mapping algorithms into architectures: Inferring the datapath and control from algorithms signal flow graph, data dependencies, datapath synthesis, control structures, critical path and worst case timing analysis, multi-function register, multiplexer optimization, concept of hierarchical system design
Logic design: Logic optimization techniques, Iterative logic arrays, Bit-sliced design, cascadable logic, power and delay minimization at logic level, logic simulation at structural level
Datapath and control design: Pipelining and parallel processing, latency, throughput, VLSI architectures for computer arithmetic algorithms: fast adders, multipliers, dividers, square root extractors, CORDIC units. Architecture for real time systems: running average computation, systolic array architectures, floating point computation units, hardware implementation of various control structures such as iterative loops, microprogrammed control techniques
ASIC vs. FPGA implementations: ASIC design approach- Decomposing a network into base functions, partitioning a network into subject graphs, obtaining matches and network cover. FPGA design approach- Look-Up Tables, Wide function multiplexers, carry chain configurations
Testable architecture: Controllability and observability, boundary scan and other such techniques, identifying fault locations, self reconfigurable fault tolerant architectures

Suggested Text/Reference Books:

1. M. D. Ercegovac and T. Lang, *Digital Arithmetic*, Morgan Kaufmann Publishers, 2004.
2. R. Katz, G. Borriello, *Contemporary Logic Design*, 2^{nd} Edition, Pearson, 2005.
3. B. Parhami, *Computer Arithmetic: Algorithms and Hardware Designs*, 2^{nd} Edition, Oxford University Press, New York, 2011.
4. C. H. Roth and L. L. Kinney, *Fundamentals of Logic Design*, Cengage Learning, Boston, 2010.
5. I. Koren, *Computer Arithmetic Algorithms*, 2^{nd} Edition, A.K. Peters Ltd., 2002.

Learning Outcomes: At the end of the course, the student shall be able to:

- Map algorithms to architectures.
- Realize the art of logic optimization in VLSI.
- Adaptively adopt different optimization strategies for varying target platforms of implementation.
- Choose the most suitable algorithm out of numerous other competing choices for hardware amenable implementation.
- Incorporate testable logic with minimal overhead.

Subject Name : VLSI for Computer Arithmetic

Subject Code	EC6L082	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Digital Electronics						

Objective of Course: Computer arithmetic is a subfield of digital computer organization. It deals with the hardware realization of arithmetic functions to support various computer architectures as well as with arithmetic algorithms for firmware/software implementation. A major thrust of digital computer arithmetic is the design of hardware algorithms and circuits to enhance the speed of various numeric operations. Thus much of what will be presented in this course complements the architectural and algorithmic speedup techniques, generally covered as part of any advanced computer architecture course. A detailed study of the theory and design of high-performance implementations of arithmetic in computers shall be taken up. Throughout the course, VLSI algorithms and relationship between implementation techniques, choice of the appropriate algorithm and logic technology shall be dealt with. The goal is to extract the benefits of both and achieve efficient and fast implementation.

Syllabus: 1. Introduction: Number systems and basic arithmetic operations 2 Sequential algorithms for multiplication and division 3. Floating-point arithmetic 4. Algorithms for fast addition: two-operand and multi-operand 5. High-speed multiplication 6. Fast division and division through multiplication 7. Square root algorithms 8. Efficient algorithms for evaluation of elementary functions 9. CORDIC algorithm and implementation 10. Logarithmic number systems 11. The residue number system; error correction and detection in arithmetic operations 12. VLSI for cryptography, cryptographic algorithms on reconfigurable hardware

Suggested Text/Reference Books:

1. I. Koren, *Computer Arithmetic Algorithms*, 2^{nd} Edition, A.K. Peters Ltd., 2002.
2. M. D. Ercegovac and T. Lang, *Digital Arithmetic*, Morgan Kaufmann Publishers, 2004.
3. B. Parhami, *Computer Arithmetic: Algorithms and Hardware Designs*, 2^{nd} Edition, Oxford University Press, New York, 2011.
4. A.R. Omondi, *Computer Arithmetic Systems: Algorithms, Architecture and Implementation*, Prentice Hall, 1994.
5. N.A. Saqib, Arturo Díaz Pérez, Cetin Kaya Koc, Francisco Rodriguez-Henriquez, *Cryptographic Algorithms on Reconfigurable Hardware*, Springer US, 2007.

Learning Outcomes: At the end of the course, the student shall be able to:

- Emphasize on the underlying computer arithmetic algorithms and actual hardware designs.

- Link computer arithmetic to other sub-fields of computing.
- Design arithmetic processors and embedded systems.
- Design arithmetic circuits tailored to special needs, rather than having general-purpose circuits.

Subject Name : Fault Tolerant Digital VLSI Systems

Subject Code	EC6L083	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Introduction to Electronics, Digital Electronics						

Objective of Course: VLSI gave fault-tolerant techniques a tremendous boost. It greatly reduced the cost of redundancy and made replication of components a practical reality for all applications, not just the exotic ones. Meanwhile, with the drop in cost of computing power, computer technology became pervasive, finding applications in virtually all areas of science, business, and the arts. The course will navigate through the design techniques that describe what is possible to do, to evaluation techniques that enable the designer to determine how well the reliability goals have been achieved.

Syllabus:
Origins of Fault-Tolerant Computing, Goals of Fault Tolerance, Applications of Fault-Tolerant Computing, Fault Tolerance as a Design Objective, Fundamental concepts in the theory of reliable computer systems design.
Faults, Errors, and Failures, Causes and characteristics of faults, fault models and error models
Design Techniques to Achieve Fault Tolerance: concept of redundancy, hardware redundancy, information redundancy, time redundancy and software redundancy.
Evaluation Techniques: Quantitative evaluation methods, reliability modelling, safety modelling, availability models, maintainability models, redundancy ratio.
Implementation techniques: software defense, protective redundancy, architectural support, Fault recovery techniques.
Coding theory: application to fault tolerant system design. Fault tolerance and reliability of multicomputer networks (direct and indirect) including fault-tolerant routing and sparing techniques. Yield and reliability enhancement techniques for VLSI/WSI array processors.

Suggested Text/Reference Books:

1. I. Koren and C. M. Krishna, *Fault-Tolerant Systems*,2^{nd} Edition, Morgan Kaufmann, 2020.
2. D. K. Pradhan (Editor), *Fault-Tolerant Computing: Theory and Techniques*, Prentice Hall, NJ, 1986.
3. B. Johnson, *Design and Analysis of Fault-Tolerant Digital Systems*, Addison Wesley, 1989.
4. A. Miczo, *Digital Logic Testing and Simulation*, John Wiley & Sons, 1987.

Learning Outcomes: At the end of the course, the student shall be able to:

- Realize highly reliable systems used in critical applications such as health, commerce, transportation, utilities, and national security.

- Realize probabilistic tools for use in analysis of reliability measures.
- Design fault-tolerant hardware and software.
- Use fault-tolerance techniques to improve manufacturing yields and design & analysis of networks.

Subject Name : VLSI CAD

Subject Code	EC6L054	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Digital Electronics						

Objective of Course: To deal with the complexity of millions of components and achieve a turn around time of a couple of months, VLSI design tools must not only be computationally fast but also should perform close to optimal. This course addresses the algorithms which facilitate electronic design automation which explores a larger design space, often under several constraints, to yield a high performance solution. to At the end of the module students are expected to be capable of employing algorithms for computer-aided design of (digital) integrated circuits, electronic systems, and other emerging platforms. These comprise: synthesis and optimization of digital circuits on logic level; simulation of digital circuits on logic level; along with efficient backend design. With a good understanding of the inner workings of modern EDA tools, students can use and develop EDA tools more effectively and efficiently.

Syllabus: High level synthesis: scheduling algorithms, allocation and binding. Representation of digital circuits by Boolean functions, Optimization of combinatorial two-level digital circuits: Quine-McCluskey; Karnaugh diagram; cube graph; resolution method; combinatorial optimization (cofactor, Boole's expansion); BDDs. Optimization of multi-level, multi-output, incompletely specified Boolean functions: Sharing of logic; finding common cubes; utilizing "don't cares"; functional decomposition. Optimization of sequential circuits: Representation of sequential circuits by FSMs; optimization of FSMs; binary coding of FSMs. Fundamental introduction to digital simulation concepts, functional simulation at architectural level, logic simulation at structural level. Circuit synthesis. Physical design automation algorithms for partitioning, floor-planning, placement, routing, design rule check, power and delay estimation, clock and power routing, layout compaction.

Suggested Text/Reference Books:

1. Sabih H. Gerez, *Algorithms for VLSI Design Automation*,John Wiley & Sons, 1999
2. De Micheli, Giovanni, *Synthesis and Optimization of Digital Circuits*, McGraw-Hill, 1994
3. S. Sait, H. Youssef, *VLSI Physical Design Automation*, McGraw-Hill, 1995
4. Gary D. Hachtel, Fabio Somenzi, *Logic Synthesis and Verification Algorithms*,Springer New York, NY, 2005
5. Bradley, Hax, and Magnanti, *Applied Mathematical Programming; Bradley*, Addison-Wesley, 1977

Learning Outcomes: Upon successful completion of the course, students should be able to:

- Understand and apply high-level synthesis techniques, including scheduling, allocation, and binding.
- Represent digital circuits using Boolean functions and optimize them using methods like Quine-McCluskey and Karnaugh diagrams.
- Perform combinatorial optimization using techniques such as cofactor, Boole's expansion, and BDDs.
- Optimize multi-level, multi-output, and incompletely specified Boolean functions by sharing logic and utilizing "don't care" conditions.
- Implement functional decomposition for the simplification of digital circuits.
- Represent and optimize sequential circuits using Finite State Machines (FSMs) and binary coding techniques.
- Grasp fundamental digital simulation concepts and perform functional and logic simulation at different levels.
- Synthesize digital circuits from high-level descriptions to gate-level implementations.
- Apply physical design automation algorithms for tasks like partitioning, floor-planning, placement, and routing.
- Estimate power consumption and delay in digital circuits, and optimize clock and power routing for enhanced performance.

Subject Name : VLSI Testing

Subject Code	EC6L055	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Digital Electronics						

Objective of Course: Testing is an integral part of the VLSI design cycle. With the advancement in IC technology, designs are becoming more and more complex, making their testing challenging. Testing occupies 60-80% time of the design process. A well structured method for testing needs to be followed to ensure high yield and proper detection of faulty chips after manufacturing. Design for testability (DFT) is a matured domain now, and thus needs to be followed by all the VLSI designers. In this context, the course attempts to expose the students and practitioners to the most recent, yet fundamental, VLSI test principles and DFT architectures in an effort to help them design better quality products that can be reliably manufactured in large quantity.

Syllabus: Introduction to Digital Testing: Test process and Test economics, Functional vs. Structural Testing, Defects, Errors, Faults and Fault Modeling (mainly stuck at fault modeling), Fault Equivalence, Fault Dominance, Fault Collapsing and Checkpoint Theorem
Fault Simulation and Testability Measures: Circuit Modeling and Algorithms for Fault Simulation: Serial Fault Simulation, Parallel Fault Simulation, Deductive Fault Simulation, Concurrent Fault Simulation, Critical path tracing, Combinational SCOAP Measures and Sequential SCOAP Measures
Combinational Circuit Test Pattern Generation: Introduction to Automatic Test Pattern Generation (ATPG), Exhaustive, random and weighted test pattern generation; aliasing and its effect on fault coverage, Standard ATPG Algorithms: D-Calculus and D-Algorithm, PODEM and FAN
Sequential Circuit Testing and Scan Chains: Ad-hoc and structured techniques, ATPG for Single-Clock Synchronous Circuits, Use of Nine-Valued Logic and Time-Frame Expansion Methods, Complexity of sequential ATPG, scan chain based sequential circuit testing: scan cell design, design variations of scan chains, Sequential testing based on scan chains, Overheads of scan design, partial scan design, LSSD, Boundary scan
Built in Self test (BIST): Introduction to BIST architecture, BIST Test Pattern Generation, Response Compaction and Response Analysis
Memory testing: permanent, intermittent and pattern-sensitive faults; test generation.
System-on-chip (SoC) testing. Low-power testing. Delay fault testing.

Suggested Text/Reference Books:

1. M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing*, Kluwer Academic Publishers, 2000.

2. N. K. Jha and S. Gupta, *Testing of Digital Systems*, Cambridge University Press, 2004.

3. M. Abramovici, M. A. Breuer and A. D. Friedman, *Digital Systems Testing and Testable Design*, Wiley-IEEE Press, 1993.

4. L-T. Wang, C-W. Wu and X. Wen, *VLSI Test Principles and Architectures*, Morgan Kaufman Publishers, 2006.

Learning Outcomes: At the end of the course, the student shall be able to:

- Apply the concepts in testing which can help them design a better yield in IC design.
- Recognize the need for systematic test methods to ensure quality and reduce cost for complex integrated circuits.
- Tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.
- Understand test generation algorithms such as PODEM.
- Learn about scan design, boundary scan, built-in self-test, and similar design-for-testability solutions.
- Gain familiarity with advanced concepts such as delay testing, test compression, diagnosis, and 3D integration.

Subject Name : SerDes Systems & Circuits

Subject Code	EC6L062	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: To provide fundamental concepts and understanding of the high speed serial communication system which is the back-bone of the modern data centers as well as any high performance system. To provide the understanding of the architecture and basic concepts of the various components of SerDes system like the channel models, and equalizers, CDR and PLL circuits; To be able to determine the parameters of these systems starting from specifications.

Syllabus: Lossless/lossy transmission lines; S-parameters, impedance matching; Overview of high-speed serializers and deserializers; Channel model, inter-symbol-interference (ISI), cross-talks; Eye diagrams and BER estimation (based on eye quality factor); Current-Mode and Voltage Mode signaling; Equalization and equalizers; Pre-emphasis (FIR) equalization for transmitters; CTLE (continuous time linear equalizers); FFE (feed-forward equalizers); Non-linear equalizers (decision-feedback equalizers); Basic circuit level blocks: Latches, flip-flops, XOR gates, muxes etc. in Current Mode Logic (CML); TSPC; Phase-locked loops (PLLs) and delay locked loops (DLLs) - Building blocks, Loop analysis, A brief overview of non-idealities in the PLLs/DLLs, Jitter and phase noise (and relationship between them), Jitter transfer functions in DLLs and PLLs; Clock and data recovery (CDR) / deserializers-Phase detectors (linear/non-linear, full-rate/nth-rate etc.) and some examples; LMS adaptation for equalizers; T-Coil for Bandwidth Enhancement.

Suggested Text/Reference Books:

1. Kyung Suk (Dan) Oh, Xing Chao (Chuck) Yuan, High-Speed Signaling Jitter Modeling, Analysis, and Budgeting, Prentice Hall, 1st Edition
2. Behzad Razavi, Design of Integrated Circuits for Optical Communications, Wiley, 2nd Edition

Learning Outcomes: At the end of the course, students must be able to

- Explain the basic concepts required to characterise a serial link
- Design and analyze current-mode and voltage mode signaling .
- Design and analyze different types of equalizer both at the transmitting and receiving end.
- Design and analyze PLLs, DLLs and CDR.

Subject Name : Parallel Systems

Subject Code	EC6L060	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: Modern PCs allow parallel execution of tasks. The efficient use of this parallelism however needs more than only multiple processor cores. The problem itself must be parallelizable. In this course characteristics of different parallel architectures and metrics of evaluation are described. Furthermore, models and languages for programming parallel computers are shown.

Syllabus: Theory of parallelism (parallel computer models, parallel specification forms and languages, performance models and calculation). Classification of parallel and scalable computer architectures (multiprocessors and multicomputers, vector computers, data flow machines, VLSI computing fields) Programmable System-on-Chip (SoC) architectures Programming of parallel computers (languages and models, design methods and compilers, optimization) Massive Parallelism: From Algorithm to Circuit Theoretical and practical exercises with computer-aided tools deepen the knowledge.

Suggested Text/Reference Books:

1. K. Hwang, N. Jotwani, *Advanced computer architecture: parallelism, scalability, programmability*, McGraw-Hill, New York, 1993.
2. M. Wolfe, *High performance compilers for parallel computing*, Addison-Wesley Longman Publishing Co., Inc., 1995.
3. A. Darte, Y. Robert, F. Vivien, *Scheduling and automatic parallelization*, Springer Science & Business Media, 2012.
4. U. Banerjee, *Loop parallelization*, Springer Science & Business Media, 2013.
5. S. Kung, *VLSI Array Processors*, Prentice Hall, 1988.

Learning Outcomes: Upon successful completion of the course, students should be able to:

- Understand various parallel computer models and parallel specification forms.
- Apply performance models to evaluate the efficiency of parallel systems.
- Classify and analyze different types of parallel architectures (multiprocessors, multicomputers, vector computers, data flow machines).
- Describe and utilize Programmable System-on-Chip (SoC) architectures.
- Program parallel computers using various languages and models.

- Employ design methods and compilers specific to parallel computing, optimize parallel programs for improved performance.
- Transition from algorithm design to circuit implementation in massively parallel systems.
- Design and implement parallel algorithms for different parallel architectures.

Subject Name : VLSI Interconnects

Subject Code	EC6L084	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Introduction to Electronics, Digital Electronics, Electromagnetic Engineering.						

Objective of Course: Interconnects are the wired connections between various devices and components in an integrated circuit. As the clock frequency and operating frequency of the electronic devices is increasing, going up to several GHz, the effects of these wired connection cannot be ignored anymore. In fact, the interconnect effects which include delays, timing jitters and cross-talk are expected to become bottleneck in further increase in the speed of electronic circuits. In this course we will investigate origin of several interconnect effects and explore techniques for electromagnetic and circuit modeling of these interconnect effects. The course is of importance for anyone interested in the high frequency circuit design and signal integrity issues in electronics and telecommunication industries.

Syllabus:

Introduction to VLSI Interconnects. Distributed RC interconnect model, Elmore delay, Elmore delay in interconnects, Elmore delay in RC tree and branched interconnects

Equivalent circuit of RC interconnect, Scaling Effects, Delay mitigation in RC interconnects, RC interconnect simulation, Inductive effects in interconnects

Distributed RLC Interconnect model (Frequency domain analysis), Transmission line equations, transfer function of an interconnect, Time-domain response of a lumped model RLC circuit

Equivalent Elmore model for RLC interconnects (Distributed model), Two-pole model of RLC interconnects from ABCD parameters, Origin of the skin effect, Effective resistance at high frequencies Equivalent circuit to simulate skin effect, Power dissipation due to interconnects, Optimum interconnect width for minimizing total power dissipation, Heating effects and thermal modelling, Compact Thermal modeling with equivalent electrical circuit

Electromigration in interconnects, Mitigation of electromigration. Capacitive coupling in interconnects. Cross-talk and timing jitters in two identical interconnects. Effects of cross-talk and timing jitters

Techniques for mitigation of cross-talk, Matrix formulation of coupled interconnects. Coupled RLC interconnects, Decoupling of interconnects by diagonalization of matrix

Analysis of coupled interconnects: Extraction of capacitance and inductance, Estimation of interconnect parameters from S parameters.

Suggested Text/Reference Books:

1. J. Davis and J. Meindl, *Interconnect Technology and Design for Gigascale Integration*, Springer Science+Business Media, LLC, 2003.

2. Jens Lienig and Matthias Thiele, *Fundamentals of Electromigration-Aware Integrated Circuit De-*

sign, Springer, 2018.

Learning Outcomes: At the end of the course, the student shall be able to:

- Realize the concepts behind RC and RLC modeling of interconnects.
- Assess the conditions at which an RLC model is required and a simple RC model does not suffice.
- Explain the physics behind EM coupling in interconnects, mathematical methods for analysis of coupled interconnects, and consequences of the coupling.
- Develop understanding of various methods of extraction of interconnect parameters from full-wave EM simulations and measurements.
- Compute and simulate the above mentioned topics.
- Comprehend cutting-edge research papers in the area.

Subject Name : Digital Design with Chisel

Subject Code	EC6L085	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	Digital Electronics/or Equivalent Subjects						

Objective of Course: Introduce students to Chisel, a hardware construction language embedded in Scala. Provide an understanding of digital design concepts and principles using Chisel. Familiarize students with the Chisel syntax, features, and constructs for hardware description. Develop practical skills in designing and implementing digital circuits using Chisel. Prepare students for applying Chisel in FPGA and ASIC design projects.

Syllabus: Introduction to Chisel: Overview of Chisel and its advantages over traditional hardware description languages; Basics of Scala programming language. Chisel Basics: Introduction to basic Chisel constructs; Combinational and sequential logic in Chisel; Writing simple Chisel programs for basic digital circuits; Finite-state machines. Advanced Chisel Constructs: Parameterized modules and generators in Chisel; Working with hierarchical designs and submodules; Use of Chisel libraries and utilities for complex designs. Chisel Testing and Verification: Introduction to testing and verification methodologies in Chisel; Writing testbenches using ChiselTest; Introduction to property-based testing with ScalaCheck. Chisel for FPGA Design: Overview of FPGA architectures and toolchains; Implementing Chisel designs on FPGAs using tools like Vivado; Hands-on lab sessions for FPGA implementation.

Suggested Text/Reference Books:

1. Schoeberl M. *Digital Design with Chisel*, Kindle Direct Publishing, 2019.
2. P. Chu, *FPGA Prototyping by SystemVerilog Examples: Xilinx MicroBlaze MCS SoC Edition.* John Wiley Sons, 2018.

Learning Outcomes: Upon successful completion of the course, students should be able to:

- Understand the principles and advantages of using Chisel for digital design.
- Write Chisel programs to describe and implement digital circuits.
- Develop testbenches and verification environments for Chisel designs.
- Implement Chisel designs on FPGAs and understand FPGA design flow.

Subject Name : SystemVerilog for Design and Verification

Subject Code	EC6L086	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course: SystemVerilog is far more than Verilog with a ++ operator. A hands-on knowledge of this rich language is critical for chip design and verification engineers.Therefore, this course will familiarize the students with syntax, features, and constructs of SystemVerilog for both RTL design and Verification. This course will also provide hands-on experience with SystemVerilog through practical exercises and projects and prepare the students for real-world applications SystemVerilog in the design and verification of digital systems.

Syllabus: Introduction to SystemVerilog: Overview of SystemVerilog and its importance in digital design and verification; Basic data types, operators, and expressions in SystemVerilog; Modules, ports, and instantiation. SystemVerilog for RTL Design: Register transfer level (RTL) design concepts; Designing combinational and sequential logic using SystemVerilog; Finite state machines (FSMs) and their implementation. Assertions and Functional Coverage: Introduction to assertion-based verification (ABV); Writing and applying assertions for design verification; Functional coverage and its importance in verification. Testbenches and Verification Environments: Overview of testbench architecture and components; Developing testbenches in SystemVerilog, Transaction-level modeling (TLM) for verification. Constrained Random Verification: Fundamentals of constrained random testing; Randomization and constraints in SystemVerilog. Universal Verification Methodology (UVM): Introduction to UVM and its key components, Building UVM testbenches for verification.

Suggested Text/Reference Books:

1. S. Sutherland, *RTL modeling with SystemVerilog for simulation and synthesis: using SystemVerilog for ASIC and FPGA design*, 2017
2. S. Sutherland, S. Davidmann, P. Flake, *SystemVerilog for design: A guide to using systemverilog for hardware design*, Springer, Switzerland, 2013.
3. A. Mehta, *SystemVerilog Assertions and Functional Coverage*, Springer, 2020.
4. C. Spear, *SystemVerilog for verification: a guide to learning the testbench language features*, Springer, 2008.
5. R. Salemi, *The UVM primer: An introduction to the universal verification methodology*, Boston Light Press, 2013.

Learning Outcomes: Upon successful completion of the course, students should be able to:

- Understand and apply the basic syntax and semantics of SystemVerilog.
- Design complex digital systems using SystemVerilog. Develop testbenches for verifying digital designs.
- Implement advanced verification techniques using SystemVerilog.
- Utilize assertions, coverage, and other verification constructs in SystemVerilog.
- Integrate SystemVerilog designs with other hardware description languages (HDLs).
- Optimize digital designs for performance, area, and power.
- Work collaboratively on digital design and verification projects.
- Debug and troubleshoot digital designs and testbenches.
- Prepare and present documentation for SystemVerilog projects.